CLAIMS

WHAT IS CLAIMED IS:

1. A method for performing testing of interconnections between components of a system comprising the steps of:

loading a first pattern into a controller pattern buffer of a controller;

transmitting the first pattern to a component of the components;

capturing the transmitted first pattern in a component capture buffer of the component;

performing a first comparison to compare the captured first pattern to the first pattern; and

identifying any interconnect faults based on the first comparison.

2. The method of claim 1 further comprising the step of preparing the component capture buffer to capture the transmitted first pattern.

3. The method of claim 2 wherein the step of preparing the component capture buffer further comprises the step of placing the component in an interconnect test mode.

4. The method of claim 3 wherein the component is a memory device.

5. The method of claim 4 further comprising the step of transferring the captured first pattern from the component capture buffer to the controller.

6. The method of claim 5 wherein the step of reading the captured first pattern is performed via a serial link.

7. The method of claim 6 wherein the step of transmitting the first pattern is performed via a control bus.

8. The method of claim 7 further comprising the step of loading a second pattern into the memory device via a serial link;
performing a memory read operation;
capturing the second pattern received from the memory device;
performing a second comparison to compare the captured second pattern to the second pattern; and
identifying any interconnect faults based on the second comparison.

9. The method of claim 8 wherein the step of performing the memory read operation is performed via a control bus.

10. The method of claim 9 wherein the step of capturing the second pattern is performed by capturing the second pattern received from the memory device via a data bus.

11. The method of claim 10 further comprising the step of loading the second pattern into the controller pattern buffer of the controller.

12. The method of claim 10 wherein the second pattern is identical to the first pattern.

13. The method of claim 2 further comprising the steps of:
loading a second pattern into a component pattern buffer of the component;
transmitting the second pattern to the controller;
capturing the transmitted second pattern in a controller capture buffer of the controller; and
performing a second comparison to compare the captured second pattern to the second pattern, wherein the step of identifying any interconnect faults is based on the first comparison and the second comparison.

14. The method of claim 13 wherein the step of loading the second pattern is performed via a serial link.

15. The method of claim 13 wherein the step of loading the second pattern is performed by loading a stored pattern from an embedded memory element of the component.

16. The method of claim 13 wherein the component is a graphics processor.

17. The method of claim 13 wherein the second pattern is identical to the first pattern.

18. A system configured to facilitate interconnect testing comprising:

a first component comprising first core circuitry, first interface circuitry, and a first communication path coupling the first core circuitry to the first interface circuitry; and

a second component comprising second core circuitry, second interface circuitry, and a second path coupling the second core circuitry to the second interface circuitry, and interconnect circuitry coupling the first component to the second component, wherein a capture buffer is coupled to the first communication path.

19. The system of claim 18 wherein a second capture buffer is coupled to the second communication path.

20. The system of claim 19 wherein the first communication path comprises a first transmit path and a first receive path, wherein the first capture buffer comprises a first transmit capture buffer coupled to the first transmit communication path and a first receive buffer coupled to the first receive communication path.

21. The system of claim 20 wherein the second communication path further comprises a second transmit communication path and a second receive communication path, wherein the second capture buffer further comprises a second transmit capture buffer coupled to the second transmit communication path and a second receive capture buffer coupled to the second receive communication path.

22. The system of claim 21 wherein the first transmit communication path further comprises a first multiplexer, the first multiplexer configured to select between a first input from the first core circuitry and a second input from a first pattern buffer coupled to the multiplexer.

23. The system of claim 22 wherein the second transmit communication path further comprises a second multiplexer configured to select between a third input coupled to the second core circuitry and a fourth input coupled to a second pattern buffer coupled to the multiplexer.

24. The system of claim 22 further comprising a serial link coupling the first component to the second component, wherein the first component is configured to allow communication of first data in the first receive capture buffer to the second component via the serial link.

25. The system of claim 22 further comprising a serial link coupling the first component to the second component, wherein the second component is configured to allow communication of second data in the second receive capture buffer to the first component via the serial link.

26. The system of claim 22 further comprising a serial link coupling the first component to the second component, wherein the first component is configured to allow communication of the first pattern from the first transmit capture buffer to the second component via the serial link.

27. The system of claim 22 further comprising a serial link coupling the first component to the second component, wherein the second component is configured to allow communication of the second pattern from the second transmit capture buffer to the first component via the serial link.

28. A memory system configured to allow interconnect testing comprising:
a memory controller; and
a memory device coupled to the memory controller, wherein the memory controller comprises core circuitry, interface circuitry, and a communication path coupling the core circuitry to the interface circuitry, wherein a capture buffer is coupled to the communication path.

29. The memory system of claim 28 wherein the communication path comprises a transmit communication path and a receive communication path, wherein the capture buffer comprises a transmit capture buffer coupled to the transmit communication path and a receive capture buffer coupled to the receive communication path.

30. The memory system of claim 29 wherein the transmit communication path comprises a multiplexer configured to select between a first input coupled to the core circuitry and a second input coupled to a pattern buffer.

31. The memory system of claim 28 wherein the memory device is coupled to the memory controller via a memory serial link, a control bus, and a data bus.

32. A system configured to facilitate interconnect testing comprising:

a first component comprising first core circuitry, first interface circuitry, and a first communication means for coupling the first core circuitry to the first interface circuitry; and

a second component comprising second core circuitry, second interface circuitry, and a second communication means for coupling the core circuitry to the interface circuitry, and interconnection means for coupling the first component to the second component, wherein a means for capturing a test pattern received from the first component is coupled to the first communication means.